REMARKS

Claims 1-55 are pending in the present application. Applicant is amending claim 46. Applicant respectfully requests reconsideration of the present application in view of the foregoing amendment and the following remarks.

I. Claim Rejections - 35 U.S.C. §102

Claims 1-4, 10-13, 17, 25, 27-31, and 46-54 stand rejected as being anticipated by U.S. Patent No. 5,749,086 to Ryan. Applicant respectfully traverses these rejections.

Applicant submits that claim 1 is not anticipated by Ryan an least by reciting "in two consecutive write cycles, at least a first and second write data ... are capable of being transferred sequentially to the memory circuit via a data bus and at least a first and second read data items ... are capable of being provided sequentially to the memory circuit via the data bus."

In this regard, Ryan discloses a synchronous memory device constructed by modifying an existing asynchronous DRAM using command signals to represent distinct command. In particular, Ryan discloses a row activation signal (RAS) which activates a process whereby, in the case of a write burst followed by a read burst (See, Ryan FIG. 19), at time T0 a write mode is selected. Ryan recites that at time T7, "a switch to read mode is initiated, ...COL n provided on the address bus is latched and a Read Burst is initiated. Following the read latency period, ... DOUT is made available on the data bus 130 at time T10." (See, Ryan, Fig. 19 and Col. 9, lines 63-67; Col. 10 lines 1-8.) Ryan therefore fails to disclose transfer of first and second write data items and first and second read data items in "two consecutive clock cycles" as recited in claim 1. Withdrawal of the rejection of claim 1 is requested.

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Claims 2-27 depend from claim 1 and are allowable for at least that reason. These dependent claims also recite additional features not disclosed by Ryan. For example, dependent claim 3 recites that each of "the first write burst operation and the first read burst operation is initiated upon an edge of a clock cycle by asserting the read/write control signal ... providing a burst address at the address bus both prior to the rising edge of the clock cycle." Claim 4 is further not anticipated by Ryan by reciting, "in two and a half consecutive clock cycles at least a third and a fourth data items ... are capable of being transferred to or from respective at least two memory blocks and at least a fifth and a sixth data items ... are capable of being transferred to or from at least two memory blocks."

Additionally, Applicant submits that dependent claim 13 further distinguishes over Ryan by reciting, "a multiplexer for receiving a clock signal and the at least first and second read data items and sequentially transferring to an output bus... [the] read data items in accordance with the state of the clock signal." Ryan, in contrast, discloses a multiplexer in which "column address buffer circuitry 112 takes a column address and provides it to a column address mux 114. The Ryan column address mux 114 also receives addressing information from an address burst counter 116..., the column address mux 114 provides a column address to a column decode circuit." (Col. 5, lines 35-44.) Thus, Ryan discloses a multiplexer that provides column addresses to a decode circuit, but fails to disclose, "a multiplexer for receiving a clock signal and the at least first and second read data items and sequentially transferring to an output bus... [the] read data items in accordance with the state of the clock signal" as recited in claim 13. Withdrawal of the rejection of claims 2-27 is requested.

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Applicant submits that independent claim 28 is not anticipated by Ryan at least by reciting, "sequentially transferring at least a first and second write data items to the memory

circuit in a first clock cycle" and "sequentially transferring at least a first and second read data items to the memory circuit in a second clock cycle, wherein the first and second clock cycles are two consecutive clock cycles." Applicant submits that Ryan fails to teach transferring first and second write data items and first and second read data items in "two consecutive clock cycles" as recited in claim 28. Accordingly, Ryan does not anticipate claim 28. Withdrawal of the rejection of claim 28 is requested.

Claims 29-37 depend from claim 28 and are allowable for at least that reason. These claims also recite additional features not disclosed by Ryan. For example, dependent claim 31 further distinguishes from Ryan for reasons similar to those set forth above with respect to claims 4 and 1. Withdrawal of the rejection of claims 29-37 is requested.

Independent claim 46, as amended, is not anticipated by Ryan at least by reciting, "receiving a first read data item ... in a first read data operation and allowing first read data item to be provided on the bus within one clock cycle after the first read operation is initiated." Ryan, however, recites that at time T7, "a switch to read mode is initiated, ...COL n provided on the address bus is latched and a Read Burst is initiated. Following the read latency period, ... DOUT is made available on the data bus 130 at time T10." (See Fig. 19, Col. 10 lines1-8.) Hence, the Ryan read latency period does not allow a read data item to be provided on the bus "within one clock cycle" after the first read operation is initiated, as recited in claim 1, but rather requires intervening clock cycles, such as at times T8 and T9. Accordingly, Applicant submits that Ryan does not anticipate claim 46. Withdrawal of the rejection of claim 46 is requested.

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Claims 47-53 depend from claim 46 and are allowable for at least that reason. These dependent claims also recite additional features not disclosed by Ryan. For example, dependent claim 47 further distinguishes over Ryan by reciting "a transmission gate for

selecting for transfer to the data bus the first read data item in accordance with the state of a clock signal." Claim 51 further distinguishes over Ryan for reasons similar to those set forth above with respect to claim 13. Moreover, Applicant submits that dependent claims 48 and 52 further distinguish over Ryan for reasons similar to those set forth above with respect to claim 3 in reference to the read operation. Withdrawal of the rejection of claims 47-53 is requested.

Independent claim 54 recites "the memory circuit is capable to receive a new read or write address in each clock cycle of the clock signal, so that consecutive read and write burst operations are capable to be performed in any order with the respective read and write addresses being received by the memory circuit in consecutive clock cycles, without any dead clock cycles therebetween." Applicant submits that claim 54 is not anticipated by Ryan for reasons similar to those set forth above with respect to claim 1. Accordingly, Applicant requests withdrawal of the rejection of claim 54. Claim 55 depends on claim 54 is allowable for at least that reason. Withdrawal of the rejection of claim 55 is requested.

II. Allowable Subject Matter

The Office Action notes that claims 14-16, 18-24, 26, and 37-45 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

In a telephone conference on August 20, 2002 between Examiner Anderson and the undersigned, Examiner Anderson noted that claim 38 is an independent claim and that claim 38 is allowable. Examiner Anderson further noted that claims 39-45 depend upon claim 38 and are also allowable.

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Applicant submits that claims 14-16, 18-24, and 26 depend, either directly or indirectly upon independent claim 1, which is allowable for at least the reasons set forth above. Applicant also submits that claim 37 depends upon independent claim 28, which is allowable for at least the reasons set forth above.

Accordingly, Applicant requests withdrawal of the objections to claims.

III. Drawings

Regarding the drawings, the Office Action states as follows.

> This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed. (Office Action, Page 2, Paragraph 1).

Applicant acknowledges the foregoing and will provide formal drawings when the application is allowed.

CONCLUSION

Applicant respectfully requests allowance of all pending claims. Should there be any questions concerning this response, the Examiner is invited to call the undersigned at (415) 217-6000.

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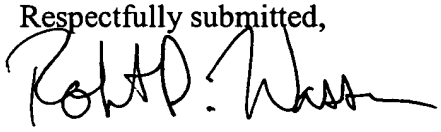
Respectfully submitted,



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ATTACHMENT A

Version of claims with markings to show changes

Claim 46 has been amended as follows. Deletions are in brackets and additions are underlined and in bold.

46. (Amended) A synchronous memory circuit comprising:

a first memory block;

a data bus for transferring data to or from the first memory block; and

an output circuit for receiving a first read data item from the first memory block in a first read operation and allowing the first read data item to be provided on the data bus [after half a] **within one** clock cycle after the first read operation is initiated.

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